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(54) Image pickup apparatus and counter circuit used therein

Bildaufnahmegerät mit darin verwendeter Zählerschaltung

Dispositif de prise d'image incorporant un circuit compteur

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Description

Background of the invention

This invention relates to an image pickup apparatus according to the preamble of claim 1.

Some image pickup apparatus such as video cameras use a solid-state image sensor composed of photodiodes and charge-coupled devices (referred to as CCDs hereafter). A driver for such a solid-state image sensor greatly affects the performance of the image pickup apparatus. As will be explained later, a prior art driver and a background driver have some problems.

An image pickup apparatus according to the preamble of claim 1 is known from EP 0 141 486. According to this document, a self scanning type image sensor for converting an optical signal to an electric signal comprises a photo transistor array composed of a plurality of phototransistors for converting an optical signal to an electric current signal; a first current switch array composed of a plurality of current switches which are connected with said plurality of phototransistors respectively; a plurality of decoder circuits each for selecting one of said plurality of current switches of said first current switch array according to a first control signal; a second current switch array composed of a plurality of current switches for selecting one of said plurality of decoder circuits according to a second control signal; a current source circuit for supplying a current to said selected one of said plurality of decoder circuits through selected one of said plurality of current switches of said second current switch array; a drive circuit for producing said first control signal applied to each of said plurality of decoder circuits and said second control signal applied to said second current switch array; and an output circuit for converting said current signal from said phototransistor array to a voltage signal.

From GB-A-1 187 868, a counter for counting an in Gray code is known comprising means responsive to incremental changes in a count and the sense of the changes to produce a first binary signal which changes in state each time the count is even and changes to the next number below and vice versa and a further signal which occurs when an even count changes to the next odd number above and vice versa, with no change in the first signal during occurrence of the further signal, a plurality of bistable counting stages, each for one digit of the code, the least significant stage being controlled by the first signal to assume a state corresponding to the state of that signal (the said state of the stage being zero if the count is zero), and control means responsive to the states of the stages and operative when said further signal occurs to change the state of one of the second or subsequent stages, such that one of those stages is changed in state when the immediately preceding stage is indicating a binary "one" and all the other preceding stages (if any) indicate a binary "zero".

SUMMARY OF THE INVENTION

It is an object of this invention to provide an improved image pickup apparatus.

This object is achieved by the features of independent claim 1.

Preferred embodiments are described in the dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a prior art image pickup apparatus.

Fig. 2 is a block diagram of the prior art image pickup apparatus.

Fig. 3 is a timing diagram showing the waveforms of signals inputted into and outputted from a binary code counter.

Fig. 4 is a block diagram of an image pickup apparatus according to a first embodiment of this invention.

Fig. 5 is a block diagram of the image pickup apparatus according to the first embodiment of this invention.

Fig. 6 is a timing diagram showing the waveforms of signals inputted into and outputted from the Gray code counter used in the image pickup apparatus of Figs. 4 and 5.

Fig. 7 is a block diagram of the Gray code counter of Fig. 5.

Fig. 8 is a timing diagram showing the waveforms of various signals in the Gray code counter of Fig. 7.

Fig. 9 is a block diagram of a prior art multi-input AND circuit.

Fig. 10 is a block diagram of an image pickup apparatus according to a second embodiment of this invention.

Fig. 11 is a frequency-domain diagram showing signals in the image pickup apparatus of Fig. 10.

Figs. 12 and 13 are time-domain diagrams which show timings at which signals change in logic state in modifications of the second embodiment of this invention.

DESCRIPTION OF THE PRIOR ART AND BACKGROUND ART

With reference to Fig. 1, a prior art image pickup apparatus includes a lens 1 and CCDs (an array of CCDs) 2. Light passes through the lens 1 and then reaches the CCDs 2, being converted by the CCDs 2 into a corresponding electric signal. The output signal from the CCDs 2 is fed to a signal processing circuit 3, being converted by the signal processing circuit 3 into a corresponding video signal of a predetermined format. The video signal is fed to a later stage, that is, a video signal circuit (not shown).

The CCDs 2 and the signal processing circuit 3 are driven by a clock signal 12 and a synchronizing signal 13 fed from a drive signal generating circuit 4. The drive

signal generating circuit 4 includes a quartz-crystal resonator 5, a clock generator 6, and a synchronizing signal generator 7.

As shown in Fig. 2, the clock generator 6 includes an oscillation circuit 8, a binary code counter 9, a decoder 10, and a latch circuit 11. The oscillation circuit 8 cooperates with the quartz-crystal resonator 5, generating a reference clock signal. The binary code counter 9 divides the frequency of the output signal from the oscillation circuit 8. The decoder 10 decodes the output signal from the binary code counter 9. The latch circuit 11 latches the output signal from the decoder 10, and feeds the clock signal 12 to the CCDs 2 as a clock signal for charge transfer.

The synchronizing signal generator 7 is basically similar in design to the clock generator 6, and includes a quartz-crystal resonator, an oscillation circuit, a binary code counter, a decoder, and a latch circuit. The latch circuit feeds a signal T3 to the signal processing circuit 3. The signal 13 is used as a synchronizing signal for the signal processing, a synchronizing signal of a television signal, a clamp pulse signal, or a blanking pulse signal.

Since the clock generator 6 and the synchronizing signal generator 7 have similar parts, it is desirable to form the clock generator 6 and the synchronizing signal generator 7 on a single chip.

A description will now be given of a conceivable design (which is not prior art to this invention) in which the clock generator 6 and the synchronizing signal generator 7 are composed of a single chip, and some of the parts of the devices 6 and 7 are used in common. In the conceivable design, the output signal 14 from the oscillator circuit 8 within the clock generator 6 is fed to the binary code counter within the synchronizing signal generator 7. Thus, the binary code counter within the synchronizing signal generator 7 continues the counting operation in response to the output signal from the oscillation circuit 8 within the clock generator 6. A portion of the output signal from the latch circuit within the synchronizing signal generator 7 is fed to the binary code counter 9 within the clock generator 6 as a control signal 15 so that the counting operation of the binary code counter 9 will be suspended during a scanning period, and that the counting operation of the binary code counter 9 will be executed during a blanking period. As a result, the output signal from the latch circuit within the clock generator 6 is fed to the CCDs 2 as a clock signal 12 for charge transfer. In addition, the output signal from the latch circuit within the synchronizing signal generator 7 is fed to the signal processing circuit 3 as a synchronizing signal 13 for signal processing.

The inventors performed experiments on the conceivable design and found the following facts. In the case where the clock generator 6 and the synchronizing signal generator 7 were formed on a common semiconductor substrate and were composed of a single chip, and where the counter for counting reference clock pulses to generate 1-H periods (one horizontal scanning periods) was composed of a binary code counter in the synchronizing signal generator 7, jitter components were given to a high-speed drive pulse signal (for example, a horizontal transfer pulse signal) at a timing where many bits of the counter simultaneously changed in digit value. As a result, a final image reproduced on the screen of a display was contaminated by vertical stripe noise of a fixed pattern.

This problem in the conceivable design will be further described. In the case where a binary code counter is fed with a clock signal having a waveform of the part (A) of Fig. 3, the binary code counter divides the frequency of the clock signal by factors of 1/2, 1/4, 1/8, ... so that the binary code counter outputs a signal of bits having waveforms of the part (B) of Fig. 3. In Fig. 3, at timings t1 and t3, five output bits of the counter change simultaneously. In addition, at a timing t2, four output bits of the counter change simultaneously.

In the conceivable design including a single chip forming both the clock generator 6 and the synchronizing signal generator 7, at such timings t1, t2, and t3 where many output bits of the binary code counter change simultaneously, a trigger-like power supply current greater than a normal power supply current flows through the circuit in the chip. The trigger-like current causes fixed-pattern noise components in the output video-information signals from the CCDs 2 and the signal processing circuit 3. The noise components result in vertical stripes in a finally-reproduced image. Further, the trigger-like current causes undesired radiation which interferes with the operation of peripheral circuits.

It was found that a similar problem arose when the counter within the clock generator 6 was composed of a binary code counter.

DESCRIPTION OF THE FIRST PREFERRED EMBODIMENT

With reference to Figs. 4 and 5, an image pickup apparatus includes a lens 1 and CCDs (an array of CCDs) 2. Light passes through the lens 1 and then reaches the CCDs 2, being converted by the CCDs 2 into a corresponding electric signal. The output signal from the CCDs 2 is fed to a signal processing circuit 3, being converted by the signal processing circuit 3 into a corresponding video signal of a predetermined format. The video signal is fed to a later stage, that is, a video signal circuit (not shown).

The CCDs 2 and the signal processing circuit 3 are driven by a clock signal 12 and a synchronizing signal 13 fed from a drive signal generating circuit 4A. The drive signal generating circuit 4A includes a quartz-crystal resonator 5, a clock generator 6A, and a synchronizing signal generator 7A. The clock generator 6A and the synchronizing signal generator 7A are composed of a single common chip.

As shown in Fig. 5, the clock generator 6A includes

an oscillation circuit 8, a Gray code counter 16, a decoder 10A, and a latch circuit 11A. The oscillation circuit 8 cooperates with the quartz-crystal resonator 5, generating a reference clock signal. The Gray code counter 16 divides the frequency of the output signal from the oscillation circuit 8. The decoder 10A decodes the output signal from the Gray code counter 16. The latch circuit 11A latches the output signal from the decoder 10A. and feeds the clock signal 12 to the CCDs 2 as a clock signal for charge transfer.

The synchronizing signal generator 7A is basically similar in design to the clock generator 6A, and includes a quartz-crystal resonator, an oscillation circuit, a Gray code counter, a decoder, and a latch circuit. The latch circuit feeds a signal 13 to the signal processing circuit 3. The signal 13 is used as a synchronizing signal for the signal processing, a synchronizing signal of a television signal, a clamp pulse signal, or a blanking pulse signal.

In the clock generator 6A, the reference clock signal fed from the oscillator circuit 8 to the Gray code counter 16 has a waveform as shown in the part (A) of Fig. 6. The Gray code counter 16 divides the frequency of the reference clock signal by factors of 1/2, 1/4, 1/8, ... so that the Gray code counter 16 outputs a signal of bits having waveforms of the part (B) of Fig. 6. As shown in Fig. 6, at each transition in the reference clock signal, only one of the bits of the output signal from the Gray code counter 16 undergoes a change. Therefore, it is possible to limit the variation of the power supply current within an acceptable range where a trigger-like power supply current is prevented from flowing through the related circuit. Thus, vertical stripe noise is prevented from occurring in a finally-reproduced image, and undesired radiation is also prevented from occurring.

As shown in Fig. 7, the Gray code counter 16 includes a clock input terminal 17 and a set of J-K flip-flops 21-26 corresponding to first to sixth counting stages (bits) respectively. The reference clock signal outputted from the oscillation circuit 8 (see Fig. 5) is fed to the clock terminals CK of the J-K flip-flops 21-26 via the clock input terminal 17.

The J terminal and the K terminal of each of the J-K flip-flops 21-26 are connected in common. The first-stage J-K flip-flop 21 are connected to a power supply terminal 18. The Q output terminal of the first-stage J-K flip-flop 21 is connected to the J terminal and the K terminal of the subsequent-stage J-K flip-flop 22. The NQ output terminal of the first-stage J-K flip-flop 21 is connected to a first input terminal of a logic gate 27 for logic decoding. A second input terminal of the logic gate 27 is connected to the Q output terminal of the second-stage J-K flip-flop 22. The output terminal of the logic gate 27 is connected to the J terminal and the K terminal of the third-stage J-K flip-flop 23.

Similarly, logic gates 28-36 for logic decoding are connected among the third-stage, fourth-stage, fifth-stage, and sixth-stage J-K flip-flops 23, 24, 25, and 26. The decoding logic gates 27-36 are composed of two-input AND gates.

Logic gates 37-42 are connected to the specific Q output terminals and the NQ output terminals of the J-K flip-flops 21-26. The logic gates 37-42 serve to equalize the number of bit or bits simultaneously subjected to changes. In addition, logic gates 43-59 for adjusting load capacitances are connected to the set of the J-K flip-flops 21-26, the set of the logic gates 27-36, and the set of the logic gates 37-42. The logic gates 37-59 are composed of two-input AND gates.

A terminal 20 leading the logic gate 42 is subjected to a positive power supply voltage or a high-level fixed voltage. Respective counting stages of the Gray code counter 16 include output terminals 60-65 corresponding to bits respectively. The output terminals 60-65 are connected to the Q output terminals of the J-K flip-flops 21-26 respectively.

Fig. 8 shows the waveforms of various signals in the Gray code counter 16 of Fig. 7. In Fig. 8, the numerals denote the waveforms of the signals inputted into and outputted from the devices represented by the same numerals of Fig. 7. Specifically, in Fig. 8, the numeral 17 denotes the waveform of the reference clock signal inputted via the input terminal 17 of Fig. 7, and the numerals 60-65 denote the waveforms of the output signals which appear at the output terminals 60-65 of Fig. 7 respectively. In addition, the numerals 27-36 denote the waveforms of the output signals from the decoding logic gates 27-36 respectively, and the numerals 37-42 denote the waveforms of the output signals from the change-bit-number controlling logic gates 37-42 respectively. In Fig. 8, the numeral 66 denotes the number of the output signals from the gates which simultaneously undergo changes.

A description will now be given of the operation of the Gray code counter 16 of Fig. 7 with reference to Fig. 8. In the case where the reference clock signal is inputted via the input terminal 17, the Q output signal from the first-stage J-K flip-flop 21 is inverted at the moment of the occurrence of each falling edge in the reference clock signal, so that the Q output signal from the first-stage J-K flip-flop 21 has a waveform 60 (21) of Fig. 8.

The Q output signal from the first-stage J-K flip-flop 21 is fed to the J terminal and the K terminal of the second-stage J-K flip-flop 22. Thus, the Q output signal from the second-stage J-K flip-flop 22 is inverted at the moment of the occurrence of each rising edge in the reference clock signal, provided that the Q output signal from the first-stage J-K flip-flop 21 is in its high-level state. As a result, the Q output signal from the second-stage J-K flip-flop 22 has a waveform 61 (22) of Fig. 8.

The NQ output signal from the first-stage J-K flip-flop 21 and the Q output signal from the second-stage J-K flip-flop 22 are inputted into the logic gate 27, and are decoded by the logic gate 27 into a pulse signal which is fed to the J terminal and the K terminal of the third-stage J-K flip-flop 23. Provided that the Q output

signal from the second-stage J-K flip-flop 22 is in its high-level state and the NQ output signal from the first-stage J-K flip-flop 22 is in its high-level state, the Q output signal from the third-stage J-K flip-flop 23 is inverted at the moment of the occurrence of each rising edge in the reference clock signal. As a result, the Q output signal from the third-stage J-K flip-flop 23 has a waveform 62 (23) of Fig. 8.

The later stages perform similar processes. Specifically, the logic gates 26 and 29 receive the Q output signal from the third-stage J-K flip-flop 23 and the NQ output signals from the first-stage and second-stage J-K flip-flops 21 and 22, decoding the received signals into a pulse signal which is fed to the fourth-stage J-K flip-flop 24. The logic gates 30, 31, and 32 receive the Q output signal from the fourth-stage J-K flip-flop 24 and the NQ output signals from the first-stage, second-stage, and third-stage J-K flip-flops 21, 22, and 23, decoding the received signals into a pulse signal which is fed to the fifth-stage J-K flip-flop 25. The logic gates 33, 34, 35, and 36 receive the Q output signal from the fifth-stage J-K flip-flop 25 and the NQ output signals from the first-stage, second-stage, third-stage, and fourth-stage J-K flip-flops 21, 22, 23, and 24, decoding the received signals into a pulse signal which is fed to the sixth-stage J-K flip-flop 26. As a result, the Q output signals from the fourth-stage and later stage J-K flip-flops 24-26, that is, the output signals induced at the output terminals 63-65, have waveforms 63-65 (24-26) of Fig. 8. In addition, the output signals from the logic gates 27-36 have waveforms 27-36 of Fig. 8.

As shown in Fig. 8, the output bit signals 60-65 from the Gray code counter 16 compose a Gray code output signal in which only one of the bits undergoes a logic state change at each transition timing. In Fig. 8, the numeral 66 denotes the number of the signals among the signals 60-65, 27-36, and 37-42 which simultaneously undergo logic-state changes. Specifically, at a first transition timing, the signal 61 changes from the low level to the high level while the signal 39 changes from the high level to the low level. Thus, at the first transition timing, the number of the signals which simultaneously undergo logic-state changes is equal to 2. At a second transition timing, the signals 60 and 27 change simultaneously in logic state, and the number of the simultaneously-changing signals is also equal to 2. At a third transition timing, the signals 62 and 38 change simultaneously in logic state, and the number of the simultaneously-changing signals is also equal to 2. Similarly, at later transition timings, the number of the simultaneously-changing signals is maintained at 2. Thus, in the Gray code counter of Fig. 7, the number of the simultaneously-changing signals is limited to 2. This is advantageous in preventing vertical stripe noise from occurring in a finally-reproduced image, and preventing undesired radiation.

The decoding logic gates 28-36 and the change-bit-number controlling logic gates 37-40 are designed so as to equalize the number of simultaneously-changing signals. Specifically, the logic gates 28 and 29 compose a 4-input AND gate which is quite different from a well-known typical 4-input AND gate shown in Fig. 9. In the well-known 4-input AND gate of Fig. 9, a lower bit I4 changes at a low frequency while a higher bit I1 changes at a higher frequency, so that there periodically occurs a timing at which both the lower bit I4 and the higher bit I1 change simultaneously. Therefore, by using the well-known 4-input AND gate of Fig. 4, it is generally difficult to equalize the number of simultaneously-changing signals. On the other hand, in the embodiment of this invention, the output signal from the first logic gate 28 is inputted into the second logic gate 29 so as to virtually compose a 4-input AND gate. This arrangement ensures that the number of simultaneously-changing signals will always be equalized. The set of the logic gates 30-32, the set of the logic gates 33-36, and the set of the logic gates 37-40 are designed similarly.

In the Gray code counter 16 of Fig. 7, the NQ output terminals of the J-K flip-flops 21-26 are connected to different numbers of the logic gates selected from the decoding logic gates 27-36 and the change-bit-number controlling logic gates 37-40. Specifically, the NQ output terminal of the first-stage J-K flip-flop 21 is connected to the five logic gates 27, 29, 32, 36, and 40 while the NQ output terminal of the second-stage J-K flip-flop 22 is connected to the four logic gates 28, 31, 35, and 39. Further, the NQ output terminal of the third-stage J-K flip-flop 23 is connected to the three logic gates 30, 34, and 38 while the NQ output terminal of the fourth-stage J-K flip-flop 24 is connected to the two logic gates 33 and 37. In addition, the NQ output terminal of the fifth-stage J-K flip-flop 25 is connected to the one logic gate 37 while the NQ output terminal of the final-stage J-K flip-flop 26 is not connected to any logic gate.

When the J-K flip-flops 21-26 are connected to different numbers of the logic gates in this manner, the load capacitances of the output lines of the respective counting stages of the Gray code counter 16 would be uneven. Such an unevenness might cause counting noise of uneven levels in response to the reference clock signal. In the Gray code counter 16 of Fig. 7, the capacitance-adjusting logic gates 43-59 are added in order to remove such an unevenness in the load capacitances of the output lines of the respective counting stages. Specifically, the logic gate 43 is provided for the second-stage J-K flip-flop 22, and the logic gates 44 and 45 are provided for the third-stage J-K flip-flop 23. The logic gates 46-48 are provided for the fourth-stage J-K flip-flop 24. The logic gates 49-52 are provided for the fifth-stage J-K flip-flop 25. The logic gates 53-57 are provided for the sixth-stage J-K flip-flop 26. According to this arrangement, the J-K flip-flops 21-26 are connected to equal numbers of logic gates so that the load capacitances of the output lines of the respective counting stages can be even. Specifically, the first-stage J-K flip-flop 21 is connected to the five logic gates 27, 29, 32,

36, and 40, and the second-stage J-K flip-flop 22 is also connected to the five logic gates 28, 31, 35, 39, and 43. The third-stage J-K flip-flop 23 is also connected to the five logic gates 30, 34, 38, 44, and 45. The fourth-stage J-K flip-flop 24 is also connected to the five logic gates 33, 37, 46, 47, and 48. The fifth-stage J-K flip-flop 25 is also connected to the five logic gates 37, 49, 50, 51, and 52. The sixth-stage J-K flip-flop 26 is also connected to the five logic gates 53-57.

The capacitance-adjusting logic gates 58 and 59 are used in processing the output signals from the change-bit-number controlling logic gates 37-42.

This embodiment may be modified in various ways. For example, the design of Fig. 7 may be modified to compose an n-bit Gray code counter where "n" denotes a natural number different from 6. In this modification, the J terminal and the K terminal of a k-th-bit J-K flip-flop are fed with an output pulse signal from a set of logic gates which cooperate to decode the Q output signal from a (k-1)-th-bit J-K flip-flop and the NQ output signals from a 1-st-bit to a (k-2)-th-bit J-K flip-flops.

In a second modification, the AND gates 27-59 are replaced by D flip-flops and Exclusive-OR gates. In a third modification, the decoding AND gates 27-36 are replaced by multi-input AND gates or other logic gates such as NAND gates. In the case where the decoding AND gates 27-36 are replaced by the NAND gates, a phase inverting process is performed at an input side or an output side. In a fourth modification, the change-bit-number controlling AND gates 37-42 and the capacitance-adjusting AND gates 43-59 are replaced by multi-input AND gates or other logic circuits.

DESCRIPTION OF THE SECOND PREFERRED EMBODIMENT

Fig. 10 shows a second embodiment of this invention which is similar to the embodiment of Figs. 4-8 except for design changes indicated hereinafter. In the embodiment of Fig. 10, Gray code counters within a clock generator 6A and a synchronizing signal generator 7A are designed so that the frequency of the occurrence of simultaneous changes of signals in the Gray code counters will be higher than a frequency band of a video signal. Further, the embodiment of Fig. 10 additionally includes a low pass filter 67 which processes the output video signal from a signal processing circuit 3. The low pass filter 67 removes high-frequency noise components from the video signal and passes only true signal components of the video signal. The output signal from the low pass filter 67 is used as an output signal from an image pickup apparatus.

As shown in Fig. 8, the output signals of respective counting stages of the Gray code counter change in logic state in synchronism with a reference clock signal 17. In addition, the output signals from logic gates 27-42 change in logic state in synchronism with the reference clock signal 17. In other words, the timing of the occurrence of simultaneous changes of signals (see the part 66 of Fig. 8) is synchronous with the reference clock signal 17. By setting the frequency of the reference clock signal 17 higher than the frequency band of the video signal, the frequency of the occurrence of simultaneous changes of signals in the Gray code counters is made higher than the frequency band of the video signal.

The period of the occurrence of simultaneous changes of signals in the Gray code counters is now represented by the character T1 as shown in Fig. 8. The frequency of the occurrence of simultaneous changes of signals in the Gray code counters is represented by the character f1. The period and the frequency have the relation as "f1=1/T1". As shown in Fig. 11, the frequency f1 is set higher than the upper limit f0 of the frequency band of the video signal. It is well-known that the frequency band of a video signal depends on the format of the video signal. For example, the frequency band of an NTSC television signal is equal to 4.2 MHz, and the frequency bands of a PAL television signal and a SECAM television signal range from 5 MHz to 6 MHz.

In this embodiment, even if simultaneous changes of signals in the Gray code counters cause noise, the frequency of the noise is higher than the frequency band of the video signal and therefore the noise is effectively removed from the video signal by the low pass filter 67.

This embodiment may be modified as follows. In a modification of this embodiment, the Gray code counters are replaced by Johnson counters, ring counters, or other counters. In this modification, when simultaneous changes of signals in the counters have periods T2 and T3 as shown in Fig. 12, the related frequencies f2 (=1/T2) and f3 (=1/T3) are set higher than the frequency band of the video signal by suitably choosing the frequency of the reference clock signal. In addition, when simultaneous changes of signals in the counters have a period T4 as shown in Fig. 13, the related frequency f4 (=1/T4) is set higher than the frequency band of the video signal by suitably choosing the frequency of the reference clock signal.

Claims

1. An image pickup apparatus comprising:

a solid-state image sensor (2) for converting light into an electrical signal;

means (5, 8) for generating a reference clock signal;

a Gray code output signal generating means for generating Gray code output signals in response to the reference clock signals;

feeding means (11A) for feeding a clock signal (12) generated from the Gray code output sig-

nals to the solid-state image sensor (2);

characterized in that

said Gray code output signal generating means is a Gray code counter means for counting pulses of said reference clock signal and for generating said Gray code output signals;

the Gray code counter means comprises a Gray code counter (16) having n one-bit counting stages (21 - 26), where n denotes a predetermined number equal to or greater than 3, with each of said counting stages (21 - 26) having a first and a second logical output, and a plurality of logic decoding means (27; 28, 29; 30 - 32; 33 - 36) including different numbers x of multi-input logic circuits (27 -36), where x denotes a respective natural number, each of said logic decoding means (27; 28, 29; 30 - 32 ; 33 - 36) being provided for feeding a logic output to an input terminal of an associated k-th-bit counting stage (21 - 26), where k denotes a natural number from 3 to n, each of said logic decoding means (27; 28, 29; 30 - 32 ; 33 - 36) being associated with a different counting stage, the logic output of a respective logic decoding means (27; 28, 29 ; 30 - 32; 33 - 36) fed to the associated counting stage being equivalent to the logic product of the first logic output of the directly preceding counting stage and the second logic output of each other preceding lower bit counting stage, each of said logic decoding means (27; 28, 29; 30 - 32; 33 - 36) which includes a respective number x of two or more multi-input logic circuits (27 - 36) comprising means for inputting and output signal of a j-th multi-input logic circuit into a (j+1)-th multi-input logic circuit, where j denotes a natural number between 1 and (x-1), and means for feeding an output signal from the x-th multip-input logic circuit to the input terminal of the associated counting stage; the Gray code counter (16) further comprising load-capacitance adjusting logic circuits (43 - 59), different numbers of said load-capacitance adjusting logic circuits (43 - 59) being connected to the output terminals of different counting stages to equalize the numbers of logic circuits composed of the multi-logic circuits (27 - 36) of the logic decoding means and the load-capacitance adjusting logic circuits (43 - 59) which are connected to the output terminals of the counting stages (21 - 26) in order to equalize the resulting load capacitances of the output lines associated with the respective output terminals of the counting stages.

2. The image pickup apparatus of claim 1, characterized by:

a signal processor (3) processing the output electrical signal of the solid-stage image sensor (2) into a video signal of a predetermined format;

said Gray code counter means comprising a first Gray code counter (16) for counting pulses of the reference clock signal and generating a first Graycode signal in response to the reference clock signal;

first means (10A) for decoding the first Gray code signal into a drive clock signal (12);

first means for feeding (11) the drive clock signal (12) to the solid-state image sensor (2) to drive the solid-state image sensor (2);

said Gray code counting means comprising a second Gray code counter (16) for counting the pulses of the reference clock signal and generating a second Gray code signal in response to the reference clock signal;

each of said first and second Gray code counters (16) comprising n one-bit counting stages (21 - 26), a plurality of logic decoding means (27; 28, 29; 30 - 32, 33 - 36) and load-capacitance adjusting logic circuits (43 - 59);

second means (10A) for decoding the second Gray code signal into a synchronizing signal (13); and

second means (11A) for feeding the synchronizing signal (13) to the signal processor (3) to control the signal processor (3).

3. The image pickup apparatus of claim 2, characterized in that it comprises a single semiconductor circuit chip including said means for generating a reference clock signal, said first and second Gray code counters (16), and said first and second decoding means (10A).

Patentansprüche

1. Bildaufnahmevorrichtung, umfassend:

einen Festkörperbildsensor (2), um Licht in ein elektrisches Signal umzuwandeln;

eine Einrichtung (5, 8) zum Erzeugen eines Referenztaktsignals;

eine Gray-Code-Ausgangssignalerzeugungseinrichtung, um Gray-Code-Ausgangssignale in Ansprechen auf die Referenztaktsignale zu erzeugen;

eine Zufuhreinrichtung (11A), um ein Taktsignal (12), das von den Gray-Code-Ausgangssignalen erzeugt wird, dem Festkörperbildsensor (2) zuzuführen;

dadurch **gekennzeichnet,** daß

die Gray-Code-Ausgangssignalerzeugungseinrichtung eine Gray-Code-Zählereinrichtung ist, um Impulse des Referenztaktsignals zu zählen und die Gray-Code-Ausgangssignale zu erzeugen;

die Gray-Code-Zählereinrichtung einen Gray-Code-Zähler (16) umfaßt, der n Ein-Bit-Zählstufen (21 - 26) aufweist, wobei n eine vorbestimmte Zahl gleich oder größer als 3 ist, wobei jede der Zählstufen (21 - 26) einen ersten und einen zweiten logischen Ausgang aufweist, und eine Vielzahl von Logik-Decodiereinrichtungen (27; 28, 29; 30 - 32; 33 - 36) umfaßt, die verschiedene Anzahlen x von Logikschaltungen (27 - 36) mit mehreren Eingängen umfassen, wobei x eine jeweilige natürliche Zahl ist, wobei jede der Logik-Decodiereinrichtungen (27; 28, 29 ; 30 - 32; 33 - 36) zur Zuführung eines Logikausganges an einen Eingangsanschluß einer zugeordneten Zählstufe für das k-te Bit (21 - 26) vorgesehen ist, wobei k eine natürliche Zahl von 3 bis n ist, wobei jede der Logik-Decodiereinrichtungen (27; 28, 29 ; 30 - 32 ; 33 - 36) einer anderen Zählstufe zugeordnet ist, wobei der Logikausgang einer jeweiligen Logik-Decodiereinrichtung (27 ; 28, 29; 30 - 32; 33 - 36), der der zugeordneten Zählstufe zugeführt wird, dem Logikprodukt des ersten Logikausganges der direkt vorausgehenden Zählstufe und des zweiten Logikausganges jeder anderen vorausgehenden Zählstufe für das niedrigere Bit entspricht, wobei jede der Logik-Decodiereinrichtungen (27; 28, 29 ; 30 - 32 ; 33 - 36), die eine jeweilige Anzahl x von zwei oder mehr Logikschaltungen (27 - 36) mit mehreren Eingängen umfaßt, eine Einrichtung zum Eingeben und Ausgeben eines Signales einer j-ten Logikschaltung mit mehreren Eingängen in eine (j + 1)-te Logikschaltung mit mehreren Eingängen umfaßt, wobei j eine natürliche Zahl zwischen 1 und (x-1) bezeichnet, und eine Einrichtung zum Zuführen eines Ausgangsaussignales von der x-ten Logikschaltung mit mehreren Eingängen zu dem Eingangsanschluß der zugeordneten Zählstufe umfaßt; wobei der Gray-Code-Zähler (16) ferner Lastkapazitätseinstellogikschaltungen (43 - 59) umfaßt, wobei verschiedene Anzahlen der Lastkapazitätseinstellogikschaltungen (43 - 59) mit den Ausgangsanschlüssen von verschiedenen Zählstufen verbunden sind, um die Anzahlen an Logikschaltungen auszugleichen, die aus den Logikschaltungen (27 - 36) mit mehreren Eingängen der Logikdecodiereinrichtungen und den Lastkapazitätseinstellogikschaltungen (43 - 59) zusammengesetzt sind, die mit den Ausgangsanschlüssen der Zählstufen (21 - 26) verbunden sind, um die resultierenden Lastkapazitäten der Ausgangsleitungen auszugleichen, die mit den jeweiligen Ausgangsanschlüssen der Zählstufen in Verbindung stehen.

2. Bildaufnahmevorrichtung nach Anspruch 1, gekennzeichnet durch

einen Signalprozessor (3), der das elektrische Ausgangssignal des Festkörperbildsensors (2) in ein Videosignal eines vorbestimmten Formats verarbeitet;

wobei die Gray-Code-Zählereinrichtung einen ersten Gray-Code-Zähler (16) zum Zählen von Impulsen des Referenztaktsignals und zum Erzeugen eines ersten Gray-Code-Signales in Ansprechen auf das Referenztaktsignal umfaßt;

eine erste Einrichtung (10A) zum Decodieren des ersten Gray-Code-Signales in ein Antriebstaktsignal (12);

eine erste Einrichtung zum Zuführen (11) des Antriebstaktsignales (12) zu dem Festkörperbildsensor (2), um den Festkörperbildsensor (2) anzutreiben;

wobei die Gray-Code-Zählereinrichtung einen zweiten Gray-Code-Zähler (16) zum Zählen der Impulse des Referenztaktsignales und zum Erzeugen eines zweiten Gray-Code-Signales in Ansprechen auf das Referenztaktsignal umfaßt;

wobei jeder der ersten und zweiten Gray-Code-Zähler (16) n Ein-Bit-Zählstufen (21 - 26), eine Vielzahl von Logik-Decodiereinrichtungen (27; 28, 29 ; 30 - 32, 33 - 36) und Lastkapazitätseinstellogikschaltungen (43 - 59) umfaßt;

eine zweite Einrichtung (10A) zum Decodieren des zweiten Gray-Code-Signales in ein Synchronsignal (13); und

eine zweite Einrichtung (11A) zum Zuführen des Synchronsignals (13) zu dem Signalprozessor (3), um den Signalprozessor (3) zu steuern.

3. Bildaufnahmevorrichtung nach Anspruch 2, dadurch **gekennzeichnet,**
daß sie einen einzelnen Halbleiterschaltungschip umfaßt, der die Einrichtung zum Erzeugen eines Referenztaktsignales, die ersten und zweiten Gray-Code-Zähler (16) und die ersten und zweiten Decodiereinrichtungen (10A) umfaßt.

Revendications

1. Dispositif de saisie d'image comprenant :

un capteur d'image à semi-conducteur (2) pour convertir la lumière en un signal électrique ;
un moyen (5, 8) pour générer un signal d'horloge de référence ;
un moyen de génération de signaux de sortie en code Gray pour générer des signaux de sortie en code Gray en réponse aux signaux d'horloge de référence ;
un moyen d'application (11A) pour appliquer un signal d'horloge (12) généré à partir des signaux de sortie en code Gray au capteur d'image à semi-conducteur (2) ;

caractérisé en ce que

ledit moyen de génération de signaux de sortie en code Gray est un moyen de compteur en code Gray pour compter les impulsions dudit signal d'horloge de référence et pour générer lesdits signaux de sortie en code Gray ;
le moyen de compteur en code Gray comprend un compteur en code Gray (16) comportant n étages de comptage à un bit (21 à 26) où n représente un nombre prédéterminé égal à trois ou supérieur à trois, chacun desdits étages de comptage (21 à 26) comportant des premier et second moyens de sortie logiques et une pluralité de moyens de décodage logiques (27 ; 28, 29 ; 30 à 32 ; 31 à 36) incluant différents nombres x de circuits logiques à entrées multiples (27 à 36) où x représente un nombre naturel respectif, chacun desdits moyens de décodage logiques (27 ; 28, 29 ; 30 à 32 ; 33 à 36) étant conçu pour appliquer une sortie logique à une borne d'entrée d'un étage de comptage associé du k-ième bit associé (21 à 26), où k représente un nombre naturel de trois à n, chacun desdits moyens de décodage logiques (27 ; 28, 29 ; 30 à 32 ; 33 à 36) étant associé à un étage de comptage différent, la sortie logique du moyen de décodage logique respectif (27 ; 28, 29 ; 30 à 32 ; 33 à 36) appliqué à l'étage de comptage associé étant équivalent au produit logique de la première sortie logique de l'étage de comptage directement précédent et de la second sortie logique de l'autre étage de comptage de bit de poids faible précédent, chacun desdits moyens de décodage logiques (27 ; 28, 29 ; 30 à 32 ; 33 à 36) qui inclut un nombre respectif x de deux ou plus circuits logiques à entrées multiples (27 à 36) comprenant un moyen pour entrer un signal de sortie d'un j-ième circuit logique à entrées multiples dans un j+1-ième circuit logique à entrées multiples, où j représente un nombre naturel situé entre 1 et (x-1), et un moyen pour appliquer un signal de sortie provenant du x-ième circuit logique à entrées multiples à la borne d'entrée de l'étage de comptage associé ; le compteur en code Gray (16) comprenant de plus des circuits logiques d'ajustement de capacité de charge (43 à 59), les différents nombres de circuits logiques d'ajustement de capacité de charge (43, 59) étant reliés aux bornes de sortie des différents étages de comptage pour égaliser les nombres des circuits logiques constitués des circuits logiques à entrées multiples (27 à 36), des moyens de décodage logique et des circuits logiques d'ajustement de capacité de charge (43 à 59) qui sont reliés aux bornes de sortie des étages de comptage (21 à 26) afin d'égaliser les capacités de charge résultantes des lignes de sortie associées aux bornes de sortie respectives des étages de comptage.

2. Dispositif de saisie d'image selon la revendication 1,

caractérisé par :

un processeur de signaux (3) traitant le signal électrique de sortie du capteur d'image à semi-conducteur (2) en un signal vidéo d'un format prédéterminé ;
ledit moyen de compteur en code Gray comprenant un premier compteur en code Gray (16) peur compter les impulsions du signal d'horloge de référence et pour générer un premier signal en code Gray en réponse au signal d'horloge de référence ;
un premier moyen (10A) pour décoder le premier signal en code Gray en un signal d'horloge d'attaque (12) ;
un premier moyen pour appliquer (11) le signal d'horloge d'attaque (12) au capteur d'image à semi-conducteur (2) pour attaquer le capteur d'image à semi-conducteur (2) ;
ledit moyen de comptage en code Gray comprenant un second compteur en code Gray (16)

pour compter les impulsions du signal d'horloge de référence et pour générer un second signal en code Gray en réponse au signal d'horloge de référence ;
chacun desdits premier et second compteurs en code Gray (16) comprenant n étages de comptage à 1 bit (21 à 26), une pluralité de moyens de décodage logique (27 ; 28, 29 ; 30 à 32 ; 33 à 36) et des circuits logiques d'ajustement de capacité de charge (43 à 59) ;
un second moyen (10A) pour décoder le second signal en code Gray en un signal de synchronisation (13) ; et
un second moyen (11A) pour appliquer le signal de synchronisation (13) au processeur de signaux (3) afin de commander le processeur de signaux (3).

3. Dispositif de saisie d'image selon la revendication 2,

caractérisé en ce qu'il

comprend une puce de circuit à semi-conducteur unique incluant lesdits moyens pour générer un signal d'horloge de référence, lesdits premier et second compteurs en code Gray (16) et lesdits premier et second moyens de décodage (10A).

FIG. 1 PRIOR ART

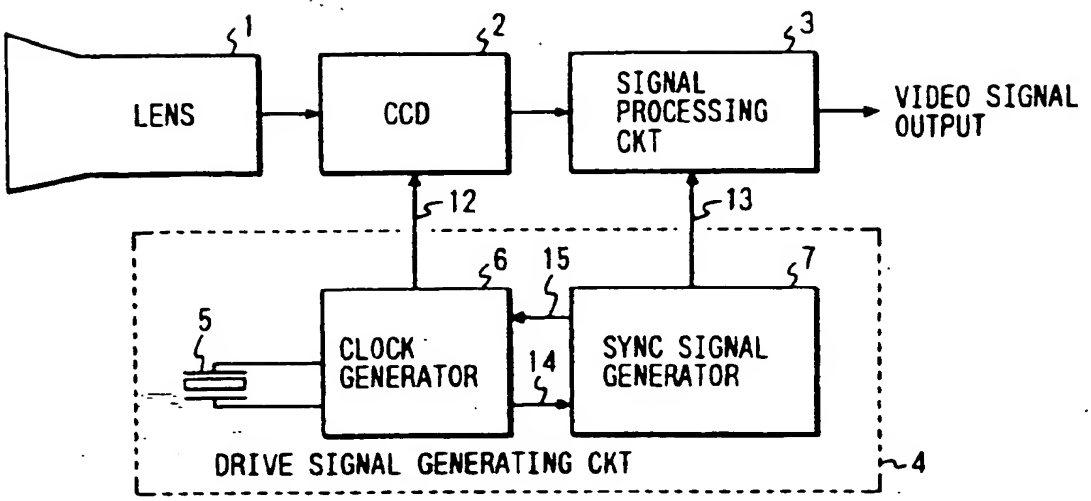


FIG. 2 PRIOR ART

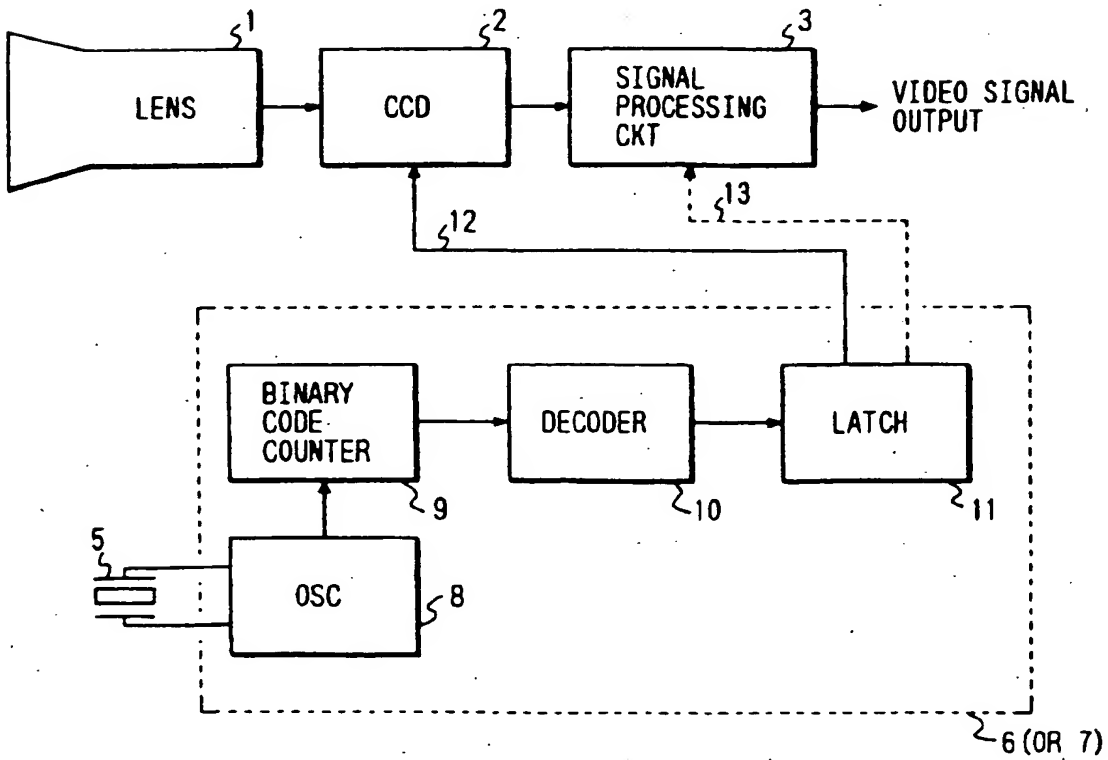


FIG. 3 PRIOR ART

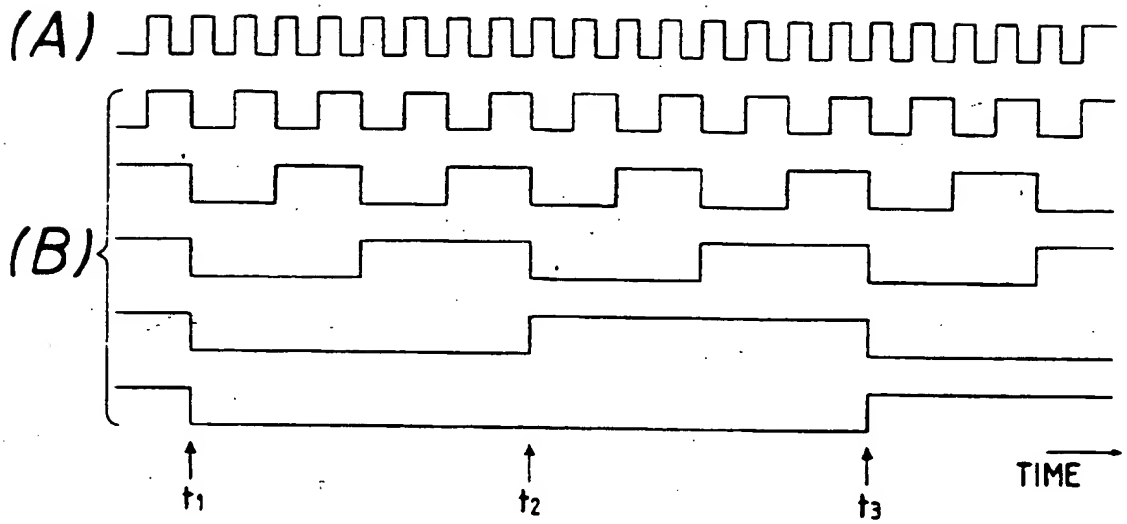


FIG. 4

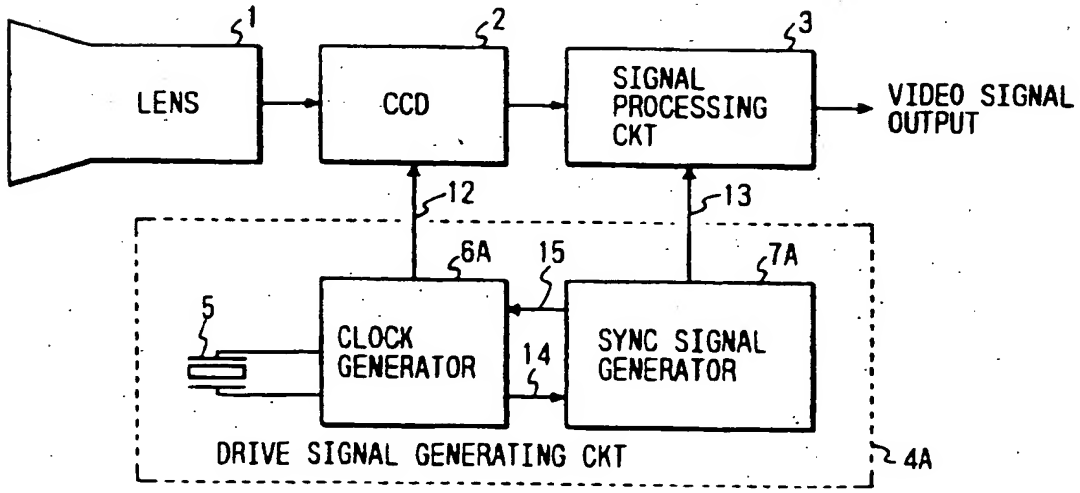


FIG. 5

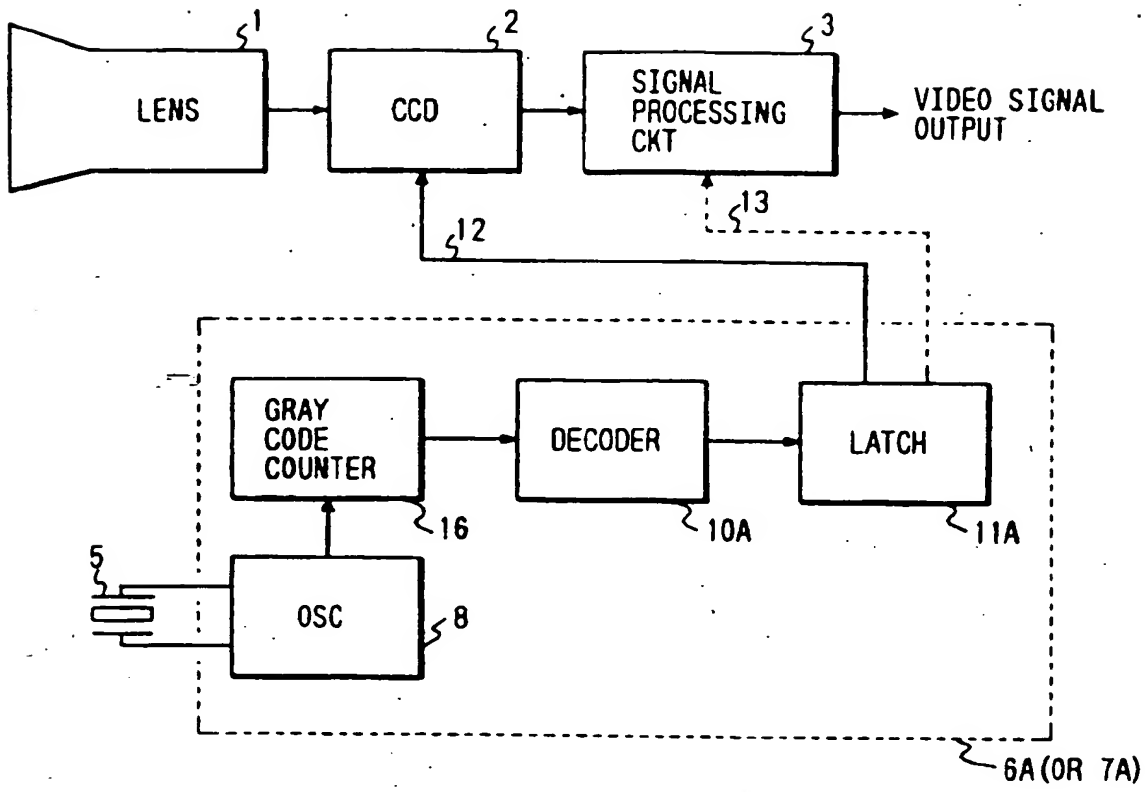

LENS
1
CCD
2
SIGNAL PROCESSING CKT
3
VIDEO SIGNAL OUTPUT
12
13
GRAY CODE COUNTER
16
DECODER
10A
LATCH
11A
5
OSC
8
6A (OR 7A)

FIG. 6

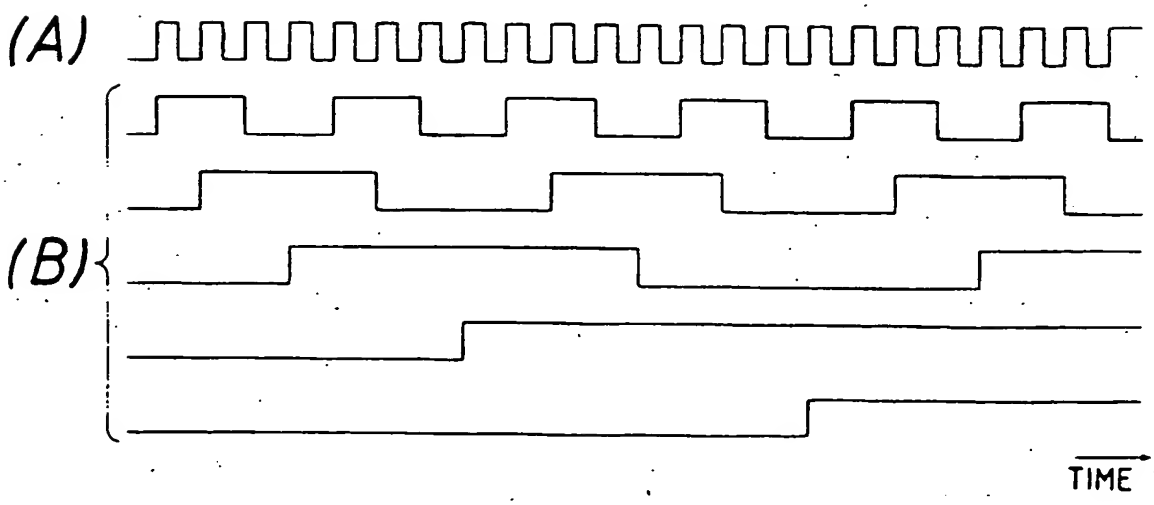
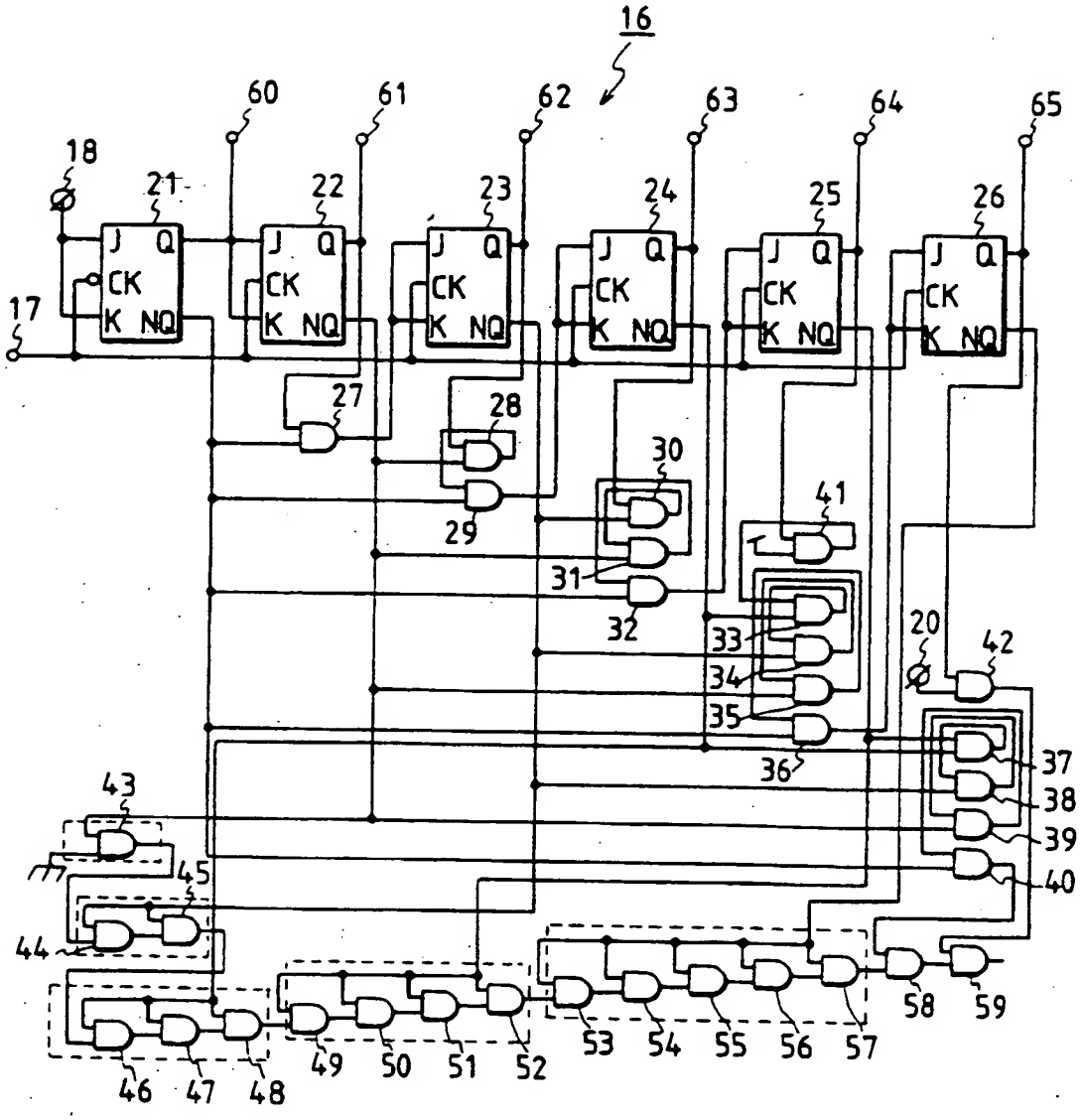

(A)
(B)
TIME

FIG. 7


16
60
61
62
63
64
65
18
21
22
23
24
25
26
J Q
CK
K NQ
17
27
28
29
30
31
32
41
33
34
35
36
20
42
37
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58
59

FIG. 8

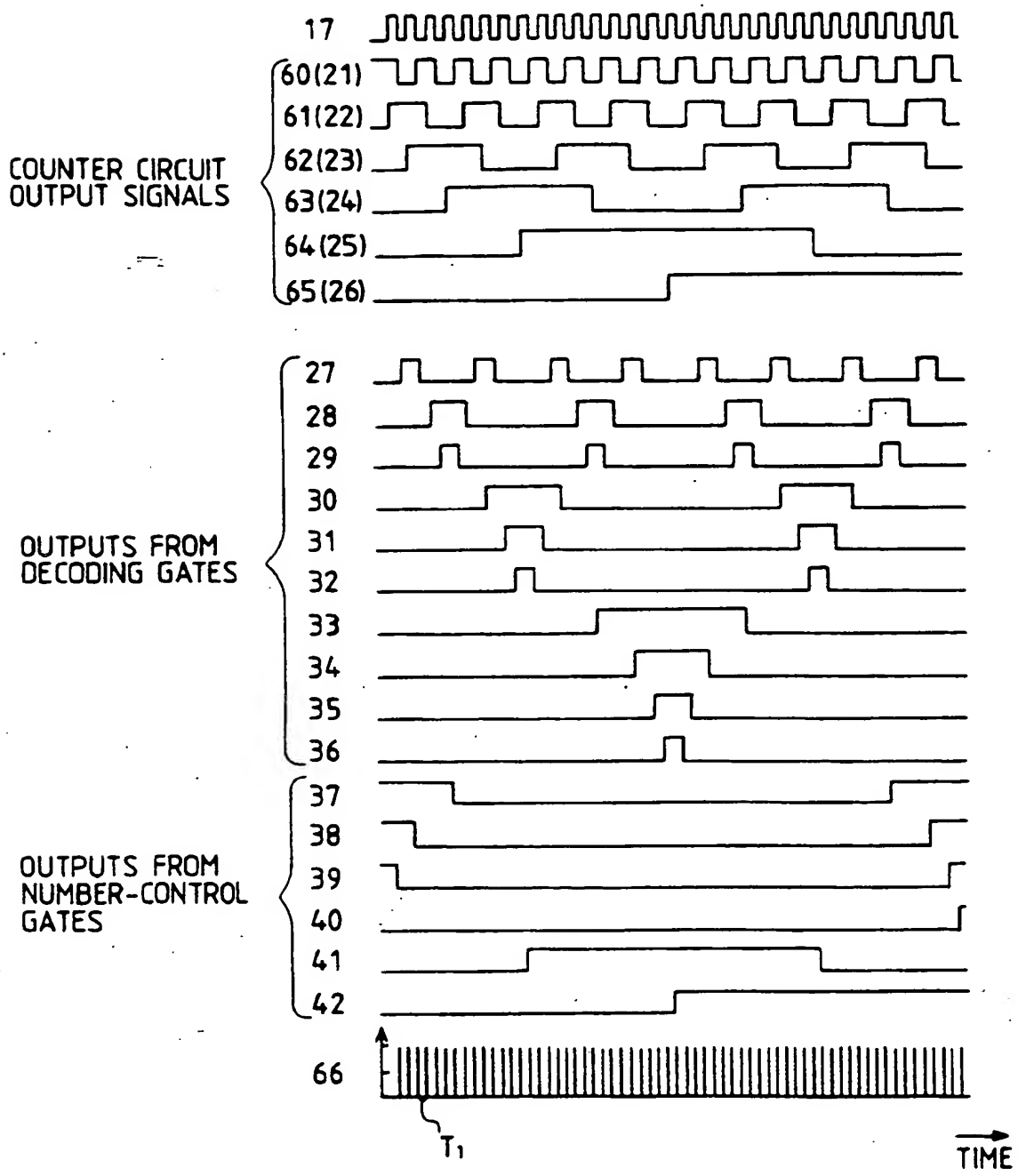
17
60(21)
61(22)
62(23)
63(24)
64(25)
65(26)
COUNTER CIRCUIT OUTPUT SIGNALS
27
28
29
30
31
32
33
34
35
36
OUTPUTS FROM DECODING GATES
37
38
39
40
41
42
OUTPUTS FROM NUMBER-CONTROL GATES
66
T1
TIME

FIG. 9
PRIOR ART

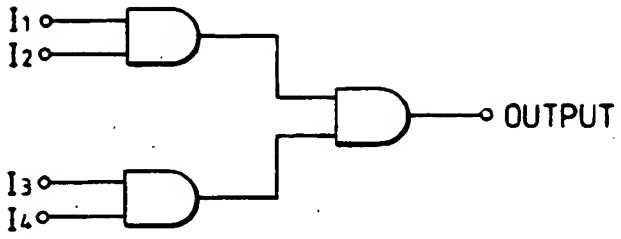

FIG. 10

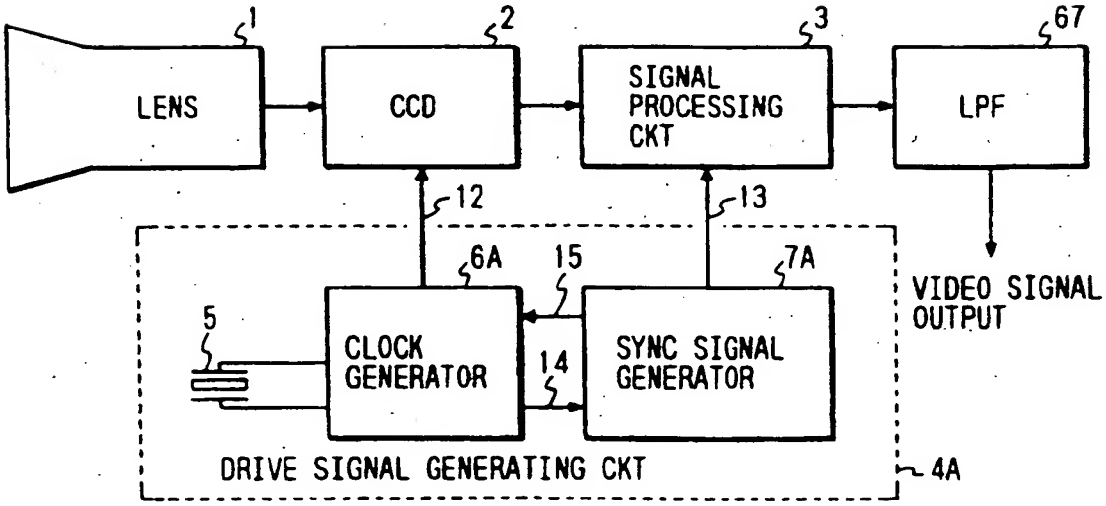

FIG. 11

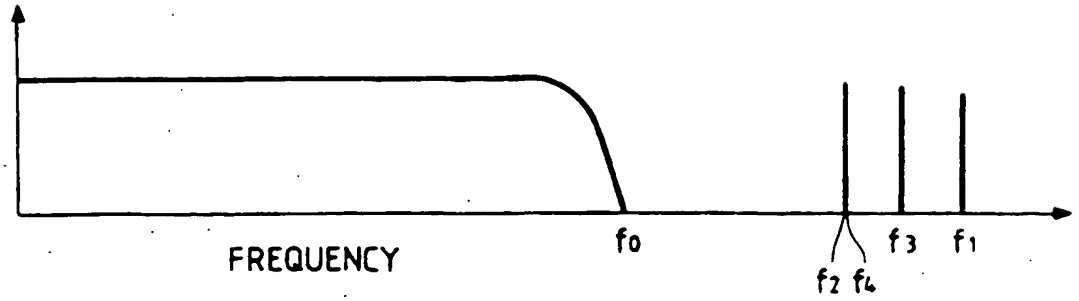

FIG. 12

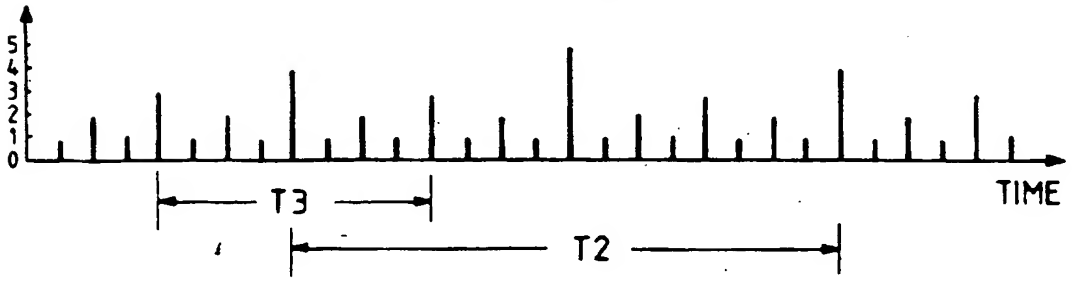

FIG. 13